

LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

5 Field of the invention

The present invention relates to a liquid crystal display, and more particularly to a liquid crystal display in which a kick-back voltage of each pixel used in an active matrix LCD (Liquid Crystal Display) is improved.

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Description of the Prior Art

In general, a structure of each pixel in a TFT-LCD (Thin Film Transistor Liquid Crystal Display) comprises one TFT of an amorphous silicon TFT and a polycrystalline silicon TFT, a
15 storage capacitor, and a pixel electrode for applying a voltage to liquid crystal. FIG. 1 is a view showing a pixel structure of in a general TFT-LCD according to the prior art. Because the pixel structure shown in FIG. 1 is a standard structure, more description about the pixel structure will be
20 omitted, while a waveform view related to an operation thereof is illustrated in FIG. 2.

As shown in FIG. 2, in the case of using a conventional pixel structure, a voltage of node P - that is, a voltage related to charge stored in the storage capacitor - is down

as much as ΔV_p (kick-back voltage) at the moment that a voltage of a gate line is transformed to a low state. This is because as a voltage of a gate line is rapidly decreased, a voltage of node P (a voltage of a pixel) is also down due to a coupling phenomenon caused by a parasitic capacitance C_{gs} between a gate electrode and a source electrode of a TFT (Thin Film Transistor). Due to this reason, a voltage dropped by ΔV_p as compared to a voltage of a data line is applied to liquid crystal. The kick-back voltage ΔV_p is generally expressed as equation 1 as follows.

Equation 1

$$\Delta V_p = C_{gs} / (C_{lc} + C_{st} + C_{gs}) \times (V_{glow} - V_{ghigh})$$

Herein, a reference character ' C_{lc} ' designates a capacitance of the liquid crystal, a reference character ' C_{gs} ' designates a parasitic capacitance between a source and a gate, and reference characters ' V_{glow} ' and ' V_{ghigh} ' designate a low voltage and a high voltage respectively applied to a gate line.

As shown in the equation 1, the kick-back voltage ΔV_p decreases a voltage of the liquid crystal, while being changed in the same direction as that of a variation of a gate voltage of a TFT. Also, since the liquid crystal

capacitance C_{lc} and the parasitic capacitance C_{gs} are changed according to an applied voltage, the kick-back voltage ΔV_p may appear as various different values according to gradation, and thus correspondingly different common voltages
5 for each different gradation are required. Therefore, a pixel structure capable of minimizing the kick-back voltage ΔV_p is required.

SUMMARY OF THE INVENTION

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Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a liquid crystal display having a pixel structure without kick-
15 back voltage.

To this end, in the present invention, proposed is a liquid crystal display capable of compensating for a kick-back voltage ΔV_p caused by a rapid change of a gate line signal by additionally constructing another gate signal line
20 having an opposite polarity with respect to a gate line signal of each pixel.

In order to accomplish this object, there is provided a liquid crystal display comprising: thin film transistors connected to intersections between a plurality of data lines

and a plurality of gate lines; pixel electrodes, each of which is connected to a source of each of the thin film transistors; common electrodes opposed to the pixel electrodes; liquid crystal injected between the pixel
5 electrodes and the common electrodes; a plurality of auxiliary gate lines corresponding to the gate lines; and first capacitors, each of which is connected between the source and each of the auxiliary gate lines.

In the present invention, a second capacitor is
10 connected between the source and each of the common electrodes.

Also, in the present invention, the polarity of the voltage applied to the auxiliary gate line is opposite to that applied to the gate line.

15 Also, in the present invention, the first capacitor has capacitance identical to that of a parasitic capacitance between the source and gate of the thin film transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

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The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a view showing a pixel structure of a general TFT-LCD according to the prior art;

FIG. 2 is a waveform view showing operation of FIG. 1;

FIG. 3 is a view showing an embodiment of a pixel
5 structure according to the prevent invention;

FIG. 4 is a waveform view showing operation of FIG. 3;
and

FIG. 5 is a view showing another embodiment of a pixel structure according to the prevent invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a preferred embodiment of the present invention will be described with reference to the
15 accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description for the same or similar components will be omitted.

20 FIG. 3 is a view showing an embodiment of a pixel structure according to the prevent invention, and FIG. 4 is a waveform view showing operation of FIG. 3.

According to an embodiment shown in FIG. 3, a liquid crystal display includes not only a plurality of first gate

lines (including an N^{th} gate line and an $(N+1)^{\text{th}}$ gate line) and a plurality of data lines (including an M^{th} data line and an $(M+1)^{\text{th}}$ data line) perpendicularly intersecting each other, but also a plurality of second gate lines (auxiliary gate lines, including an N^{th} gate bar line and an $(N+1)^{\text{th}}$ gate bar line) corresponding to the first gate lines, respectively. Also, liquid crystal is connected between ground and the source of a TFT, in which the gate of the TFT is connected to a first gate line and the drain of the TFT is connected to a corresponding data line, and a first capacitor C1 is connected between the source and a second gate line.

As shown in FIG. 3, one gate line and one data line are connected to a TFT for each pixel, and one capacitor C1 is connected between one gate bar line and node P (pixel electrode). Herein, a signal of an opposite polarity with respect to a signal of a corresponding gate line is applied to the gate bar line (see FIG. 4). In an embodiment of the present invention, it is preferred that the capacitor C1 is constructed so as to have the same capacitance as the parasitic capacitance C_{gs} between the source and the gate of the TFT.

In the case of a pixel structure shown in FIG. 3, it is possible to compensate for a kick-back voltage caused by the effect of a parasitic capacitance C_{gs} with the capacitor C1,

and the equation of the kick-back voltage ΔV_p of the case is represented as follows.

Equation 2

$$\Delta V_p = C_{gs} / (C_{lc} + C_{st} + C_{gs}) \times (V_{glow} - V_{ghigh}) +$$

$$C_l (C_{lc} + C_{st} + C_{gs}) \times (V_{ghigh} - V_{glow})$$

As shown in the equation 2, if $C_l = C_{gs}$, then the kick-back voltage ΔV_p becomes '0' theoretically. Also, even though other parasitic capacitances existing at the pixel electrode is considered, the pixel structure according to an embodiment of the present invention can minimize the kick-back voltage ΔV_p . Therefore, 0V or a much lower DC voltage than a voltage V_{com} of a conventional common electrode can be applied to the lower electrode of the liquid crystal, so that it is possible to decrease a dynamic range of the data line voltage.

FIG. 5 is a view showing another embodiment of a pixel structure according to the prevent invention.

As shown in FIG. 5, the pixel structure according to another embodiment of the present invention includes a storage capacitor C_{st} connected parallel to the liquid crystal, in addition to a capacitor C_l described in FIG. 3. The storage capacitor C_{st} not only decreases the kick-back

voltage ΔV_p but also prevents the liquid crystal voltage from decreasing due to current leakage in the liquid crystal or current leakage which may be caused when the gate of a TFT is in a turn-off state, thereby increasing the voltage-holding ratio (VHR).

As described above, in the case of using a liquid crystal display having a pixel structure according to embodiments of the present invention, even if the voltage of a gate line goes down rapidly, it is possible to minimize the variation width of a pixel voltage. Therefore, as compared to the prior art, the liquid crystal display according to the present invention has advantages in that a dynamic range of data line voltage is lower, the adjustment of the common voltage V_{com} is unnecessary, a display problem of 30Hz flicker caused by the kick-back voltage ΔV_p can be solved, and so forth.

Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.